AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 10, as follows:

FIG. 13 shows the structure of a conventional clock and data recovery circuit. From a reference clock (Ref CLK), multi-phase clocks (multiphase outputs), having an equally-spaced phase difference are generated by a voltage controlled oscillator (VCO) 51 of a phase locked loop (PLL). The VCO 51 is comprised of a ring oscillator of an analog circuit configuration, made up of an odd number of inverter circuits, connected in a ring topology. Multi-phase clocks with an equally spaced phase difference are output in a differential mode from differential inverter circuits of the respective stages making up the ring oscillator. An input data DATA is provided in common to data terminals of plural flip-flops 52 (F/F1 to F/F8) and respective multi-phase clock output from the VCO 51 are fed to clock terminals of the flip-flops 52 (F/F1 to F/F8) which sample the data DATA with rising or falling edges of clock signals and output the sampled data. The clock and data recovery circuit also includes a counter 53 which receives output data output from the plural flip-flops 52 (F/F1 to F/F8) to ~~counts~~ count up and down logic values of the output data, and a filter 55 which time-averages the output of the counter 53 over a preset time constant. An output voltage of the filter 55 is fed to the voltage-controlled oscillator (VCO) as its control voltage. Part or all of the outputs of the flip-flops 52 and one-phase clock output from the VCO 51 are output as data and clocks, respectively. The outputs of the plural flip-flops 52 (F/F1 to F/F8) are obtained on sampling the data DATA with clocks having phases shifted by a equal value and a sampling waveform which is equivalent to that of sampling the data with a frequency equal to eight times the frequency of the reference clock, is obtained, with the clock timing of a flip-flop, an output

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value of which does not coincide with the output value of the neighboring flip-flop representing a transition point of the data DATA.

Please amend the paragraph beginning at page 2, line 14, as follows:

If a clock has a delay with respect to the data transition point, that is if the latch timing is delayed, the count value of the counter 53 is incremented to advance the clock phase, whereas, if the clock leads with respect to the data transition point, the count value of the counter 53 is ~~decrement~~ decremented to delay the clock phase with respect to the data transition point. Meanwhile, the counter 53 may be made up of a charge pump (CP) which charges a capacitor with constant current when the output values of the plural flip-flops 52 (F/F1 to F/F8) are of logic 0 and discharges the capacitor with the constant current when output values of the plural flip-flops 52 (F/F1 to F/F8) are of logic 1.

Please amend the paragraph beginning at page 4, line 11, as follows:

The interpolator 30 (phase interpolator) of FIG. 14 is made up of an analog circuit shown in FIG. 15. Referring to FIG. 15, this phase interpolator includes N-channel MOS transistors MN61, and MN62, forming a first differential pair, the sources of which are connected in common to a first constant current source CS1, the gates of which receive differentially clocks IN1 and IN1B, outputs pair of which are connected to one end of a first load (a common drain of P-channel MOS transistors MP61 and MP62 connected in parallel) and to one end of a second load (a common drain of P-channel MOS transistors MP63 and MP64 connected in parallel). The phase interpolator also includes N-channel MOS transistors MN63, and MN64, forming a second differential pair, the sources of which are connected in common to a second constant current source CS2, the gates of which receive differentially clocks IN2 and IN2B, outputs pair of which are connected to one end of a first load (a common

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drain of P-channel MOS transistors MP61 and MP62 connected in parallel) and to one end of a second load (a common drain of P-channel MOS transistors MP63 and MP64 connected in parallel). From the outputs pairs connected in common of the first and second differential pairs are output ~~an output~~ signals OUT and OUTB having the phases of the weighted sum of the two input clocks. In this phase interpolator, digital weight codes ictl (16 bits of b[0] to b[15]) are fed to first and second constant current sources CS1 and CS2 to vary the current values of the first and second constant current sources CS1 and CS2, for conversion to the phase of the output clock. That is, the number of the constant current source transistors MN6B.sub.1 to MN6B.sub.15 is selected by the turning on/off of the N-channel MOS transistors MN6A.sub.1 to MN6A.sub.15, the gate terminals of which receive 16 bits b[0] to b[15], respectively, to vary the current value.

Please amend the paragraph beginning at page 5, line 15, as follows:

On the other hand, Publication 3 (ISSCC 1999 p.p. 180 to 181 "A2BParallel 1.25 Gb/s Interconnect I/O interface with Self Configurable Link and Plesiochronous Clocking") discloses a configuration, shown in FIG. 16, as a phase interpolator. Referring to FIG. 16, an output current of a current output type configuration which outputs an output current proportionate to the control circuit Ict1 is mirrored by a first current mirror circuit (MN74, and MN75), and the mirrored current is received by a second current mirror circuit (MN73, and MN74), an output mirror current of which is fed to a differential pair circuit which receives as inputs the differential clock inputs IN, and INB. The differential pair circuit is provided with the current from the constant current source transistor MN73 forming the second output end of the first current mirror circuit (MN74, and MN75) and clocks OUT, and OUTB, corresponding to phase shifted versions of the clocks IN, are output at the output nodes of the differential pair

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circuit. Meanwhile, the differential pair circuit includes N-channel MOS transistors MN71, and MN72, the sources of which are connected in common to a constant current source transistor MP73 and the gates of which are fed with differential clock pairs IN, and INB, and P-channel MOS transistors MP71, and MP72, the sources of which are connected in common to the drain of an output transistor MP74 of the second current mirror circuit, the gates of which are fed with differential clocks IN, and INB and the drains of which are connected to the drains of the N-channel MOS transistors MN71, and MN72. Outputs OUT, and OUTB are taken at the drains of the of the N-channel MOS transistors MN71, and MN72. ~~Aeross~~ Connecting the drains of the N-channel MOS transistors MN71, and MN72 and [[the]] ground are ~~connected~~ capacitances C1, and C2, respectively, whereas, ~~aeross~~ between the drains of the N-channel MOS transistors MN71, and MN72, ~~are connected~~ transistors N-channel MOS transistors MN76 and MN77 are connected in series with each other. When the N-channel MOS transistors MN76 and MN77 are turned on, the outputs OUT, and OUTB are charged to an intermediate potential VDD.

Please amend the paragraph beginning at page 16, line 11, as follows:

For further explaining the above-described embodiment of the present invention in detail, a preferred embodiment of the present invention is now explained. FIG. 1a shows the structure of an embodiment of the present invention. Referring to FIG. 1a, a clock and data recovery circuit in accordance with one embodiment of the present invention includes a phase shift circuit 101, which receives eight-phase clocks and is adapted for outputting eight sets of clocks having phases being shifted, a plural number of D-type flip-flops 102 (F/F1 to F/F8), which receive at clock input terminals thereof the clock signal output from a phase shift circuit 101, receive [[an]] input data DATA at data input terminals thereof and are adapted for

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sampling [[the]] input data DATA with the rising edge of the clock, a counter 103 for upcounting and downcounting a count value in case of the output of the plural D-type flip-flops 102 being at logic 0 or at logic 1[[ ]], respectively, a filter 105 for time averaging the output of the counter 103, a decoder 106 for decoding the output of the filter 105, and a selector (selection circuit) 104 receiving one-phase clock output from phase shift circuit 101 and output data of the plural D-type flip-flops 102 (F/F1 to F/F8) to output selected sets (one-phase clock and sampled output data) in parallel based on the selection control signal. In FIG. 1a, the selector 104 receives outputs of D-type flip-flops F/F1, F/F3, F/F5 and F/F7 as inputs among the plural D-type flip-flops (F/F1 to F/F8). Alternatively, outputs of all D-type flip-flops F/F1 to F/F8 may be fed to the selector 104.

Please amend the paragraph beginning at page 17, line 10, as follows:

The D-type flip-flops 102 (F/F1 to F/F8) sample the input data DATA with the rising (or falling) edge of the clocks CLK1 to CLK8 output from the phase shift circuit 101 (see FIG. 1b). From an output of the plural D-type flip-flops 102 (F/F1 to F/F8), such as "00001111", there is obtained waveform data on sampling the input data at a sampling period corresponding to one-eighth of the clock period. The input data undergoes a transition at a change point of output values of neighboring D-type flip-flops 102. The counter 103 counts outputs of the plural Dtype flip-flops 102 and the resulting count values are smoothed by the filter 105 at a preset time constant to manage control as to whether or not the phase of clocks supplied to the plural D-type flip-flops is [[to be]] advanced or delayed, and hence clocks and data locked to the input data DATA are output.

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Please amend the paragraph beginning at page 20, line 7, as follows:

The control signal Cnt[0:7] may be set by an output of a frequency detection circuit which detects the frequency of the clock signal. Alternatively, the control signal Cnt[0:7] may be determined [[y]] by setting the resistor or the dip switches to a desired value depending on the application. The frequency range that can be coped with may be enlarged by varying the capacitance value appended to the node N1 by the control signal Cnt[0:7].

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